REMARKS

Claims 5 and 6 have been cancelled, claim 21 - 22 have been amended, and a new claim 32 has been added to further protect the invention. The cancellation of claim 6 and the amendment to claim 22 obviate objections to these claims. The amended claims 21, 22 and 32 are all directed to a semiconductor device having primary and secondary semiconductor chips bonded to each other to form a chip-on-chip structure that is put in a package.

Claim 21 clarifies that the primary semiconductor chip has a primary functional bump and a primary dummy bump, the heights of which are substantially equal to each other. Claim 21 further clarifies that the secondary semiconductor chip has a secondary functional bump and a secondary dummy bump, the heights of which are substantially equal to each other. The secondary bump does not serve for electrical connection between internal circuits of the primary and secondary semiconductor chips, but does serve for absorption of a force exerted on the secondary semiconductor chip. The area of being joined or contact area of the primary and secondary dummy bumps extends over an entire active region of the mating surface of the secondary semiconductor chip.

Such a structure is advantageous in that the area over which the primary and secondary dummy bumps are joined is large enough to cover the entire active region of the secondary semiconductor chip, thereby protecting the active region from an external force or stress-strains that may occur when packaging with a sealing resin, for example. That is, the secondary semiconductor chip can be prevented from experiencing deformation caused by a mechanical pressure or thermal expansion, whereby deterioration of device characteristics is effectively prevented.

Support for the amendments to claim 21 will be found in the original disclosure, from page 29, lines 16 to page 33, line 20.

The newly added claim 32 is directed to a feature that had been specified in claim 21 prior to its deletion in the present amendments, specifically that at least one of the primary and secondary semiconductor chips includes a low impedance portion and the primary and secondary dummy bumps are electrically connected to the low impedance portion.

The Examiner rejected claims 5, 6, 21 and 22 under 35 USC 102(b) as being anticipated by *Takao* (JP58-091646). Claims 5 and 6 have been canceled and claims 21 and 22 have been amended. It is submitted that the rejection is inapplicable to amended claims 21 and 22.

Takao discloses a semiconductor device that has an electric insulating board 1, and a semiconductor chip 3 that is flip-chip-bonded onto the electric insulating board 1. However, *Takao* fails to disclose a chip-on-chip structure that is housed in a package. Therefore, *Takao* naturally fails to teach or suggest the problems to be solved by the present invention, that is, the deformation of a secondary semiconductor chip when packaging the chip-on-chip structure.

According to the present invention as defined in claim 21, the primary and secondary semiconductor chips are bonded to each other to form a chip-on-chip structure, and the primary and secondary semiconductor chips have dummy bumps on their opposing surfaces. The opposing dummy bumps are bonded to each other so that the area over which they are joined extends over the entire active region of the secondary semiconductor chip. The dummy bumps have a height that is substantially equal to the height of the functional bumps; therefore, the dummy bumps effectively absorb an external force exerted on the chip-on-chip structure. Such a structure and advantages are neither taught nor suggested by *Takao*. Claim 21, and claims 22 and 32 depending therefrom therefore are deemed clearly to be patentable over *Takao,* and the rejection accordingly should be withdrawn.

The Examiner also rejected claims 5 and 21 under 35 USC 102(a) as being anticipated by *Yano et al.* (US Patent No. 5,909,058). Claim 5 has been

canceled and claim 21 has been amended as discussed above. It is submitted that the rejection is inapplicable to amended claim 21.

Yano et al. disclose an arrangement that has a multi-layered mounting substrate 20, a supporting substrate 11 composed of ceramics substrate mounted on the substrate 20, and a semiconductor chip 14 bonded and mounted on the supporting substrate 11. However, Yano et al. fail to disclose the features of the primary and secondary semiconductor chips discussed above. *Yano et al.* also fail to disclose a chip-on-chip structure that is housed in a package. It is therefore clear that the features recited in amended claim 21 are neither taught nor suggested by *Yano et al.* Claim 21, and claim 32 depending therefrom, therefore are deemed clearly to be patentable over *Yano et al.,* and the rejection accordingly should be withdrawn.

Based on the above, it is submitted that the application is in condition for allowance and such a Notice, with allowed claims 21, 22 and 32, earnestly is solicited.

Respectfully submitted,

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Certification Under 37 C.F.R. §1.8 (if applicable)

I hereby certify that this Amendment is being deposited with the United States Postal Service as First Class Mail under 37 C.F.R. §1.8 on this **October 12, 2005** and addressed to the Commissioner of Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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